

Secured Failure Analysis Methodology for Accurate Diagnostic of Defects in GaN HEMT Technologies

J.G. Tartarin, D. Saugnon, L. Bary, J. Graffeuil

Abstract— III-V wide bandgap disruptive technology is positioned as a leader for high power components operating at high frequency or under switch mode conditions of operation. Further investigation to address elevated junction temperatures of these transistors would elevate the maturity of this technology to higher levels of performances. When considering analog RF applications, more than two decades of studies have laid the basis for the main technological process. However, if failure signatures and their associated defects become problematic and which are likely to be understood as individual problems, the global failure behavior in active high frequency analog devices still poses challenges which need to be overcome. This paper directly contributes to failure analysis studies on GaN technologies by providing a methodology for ensuring the validity of a stress analysis. This procedure is also suitable for a single stress test campaign, whereas several accelerated life tests are usually needed to separate concurrently proceeding effects. This methodology is based on the use of non-destructive and eventually destructive characterization techniques, as well as electrical TCAD modelling.

Index Terms— Failure analysis methodology; GaN HEMT; Reliability; TCAD; Transient & frequency characterization;

I. INTRODUCTION

RELIABILITY studies of solid state technologies have made possible the development of numerous useful tools and methods to identify degradation signatures and to correlate multiple experiments. Revealed failure mode mechanisms have raised the mastering of technological processes, up to the critical technology readiness level (main gate TRL 5 to 6) needed to secure market supplies (with specific requirements according to the targeted missions, as different as space technologies or generic off-the-shelf mainstream technologies). Well established technologies such as silicon and gallium arsenide are largely employed, and their qualification procedures are well classified by the establishment of reliability standards. However, the qualification procedures for new emerging wide bandgap nitride technologies such as gallium nitride (GaN), cannot be addressed in a similar manner to silicon and gallium arsenide.

High electron mobility transistor (HEMT) active devices based on GaN technologies are now reaching a sufficiently high TRL which allows various market segments to be targeted and exploited. A major application for analog GaN devices is in the high-power amplification of radio frequency (RF) signals as used in wireless communication systems (base station and backhaul cellular systems), defense and military systems (radar, jamming, counter-measure and guided weapon systems), broadcast and communication satellites (SatCom). In these various market segments, different categories of application feature the same trends regarding the required performance, reliability, cost, size/weight as well as legacy considerations. When considering the manufacturing foundries and brokers, winning the innovation race in terms of performance cannot be dissociated from providing customers with highly reliable devices. More than twenty industrial laboratories are engaged in the manufacture of GaN HEMT's for RF applications, and a summary of long-term accelerated tests on Nitride HEMT's carried out by some of these technology brokers can be found in [1]. A literature survey revealed that over the past few decades, channel junction temperature has been improved as shown by G. David (an improvement in mean time to failure (MTTF) by more than a factor of 10^6 from 2007 to 2014 at 150 °C, 175 °C and 200 °C [2]). These advances were achieved due to sustained efforts into technological improvement, accompanied by a better understanding of the failure signature in GaN devices. However, the complexity of the root causes of the defects in the devices must still be understood to force these GaN transistors to perform close to their theoretical limits. Parameters involved in the reliability of the devices are related to the design, processing and packaging steps in the manufacturing process. Large variations, as shown in the literature, exist in the physical structure of devices (small or large device, wafer or die level, packaged or naked die). According to a low or high value of TRL, studies during the process improvement phase focus more on the wafer level and naked die structures, whereas packaged devices will be more representative for qualification steps. The abundant literature concerning this challenging domain of study, reveals that a large variety of papers is dedicated to specific failure analysis studies in GaN devices. Some papers

This work was supported in part by GaNEX Grant (ANR-11-LABX-0014), ANR ReaGAN, ANR Genghis Khan and other collaborative projects.

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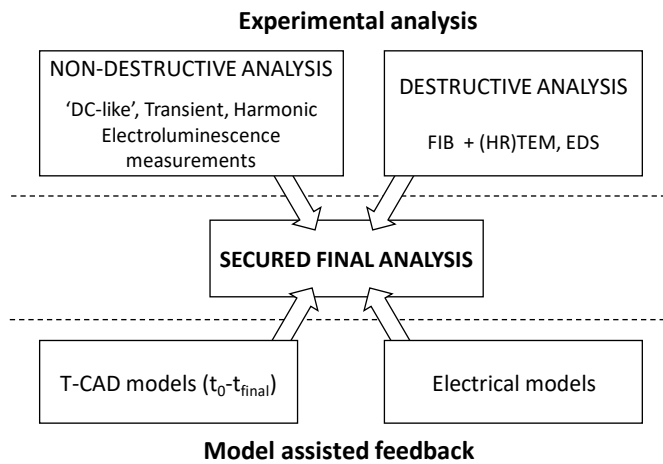


Fig. 1. Cross interpretation of non-destructive and destructive studies with electrical models for secured stress analysis. Characterizations are performed on virgin (or initial measurement) and stressed (or final measurement) devices, with possible intermediate measurements. Physical origins of the defect can be assessed, and limits of operation can be defined closely related to the stress conditions.

propose new analysis tools, some present a methodology for failure analysis [3][4][5][6][7] or some propose a general overview concerning the reliability in GaN devices [8][9][10]. Usually, the identification of a complex failure signature is achieved by performing various stress campaigns under changing conditions in order to separate competing effects of mechanisms proceeding to a failure signature. This approach is time-consuming and is not always applicable for studies featuring only one batch of stressed samples. This last study case represents a situation where it is necessary to get numerous parameters from a unique equation, which is impossible if a single analysis tool is used.

In this paper we propose a methodology suitable for identifying various defects which are revealed under multi-factor stressing conditions. That is, DC biasing with varying temperature and pulsed/continuous wave (CW) RF signals. As stated previously, a large set of experimental workbenches and dedicated models are needed to ensure a realistic and secured diagnostic concerning the failure mechanisms occurring in such technologies, and to establish their physical links. Lastly, a single stress campaign will not allow the extraction of any activation energy, and at least three stress campaigns at different temperatures will be needed to extract such parameters from an Arrhenius plot. It must be noted that Arrhenius plots are not considered to accurately account for GaN technology reliability predictions, even by using scaling factors [4], and a better knowledge of the concurring defects is more prone to define security operating areas for circuit design.

The proposed methodology, and the associated experimental tools or stress workbenches, has been attested and proven over several foundries, and over a large set of DC or RF stresses. Fig.1 summarizes the structure on which the methodology is based. It makes use of experimental analysis and of modelling techniques targeting the final diagnostic on root failure mechanisms.

This paper is divided in four main sections: following this

first introductory section, the second section presents the largely accepted stress conditions and tests, the experimental stress workbench developed in our laboratory and RF stress tests at various output power compression points. In the third section, the experimental diagnostic tools used for the reliability studies are presented, including a highlight on their complementarity, that is, the main measurements performed versus time, frequency or temperature. Finally, section four presents the development of electrical models (dynamic large signal models for circuit design and reliability analysis and TCAD models for physical acceptability of the diagnostic). The last two sections also summarize the main achieved results and conclude about the need to use a robust methodology for reliability studies of III-N technologies.

II. STRESS CONDITIONS AND TESTS

A. Main stress tests towards process improvement and process qualification

According to the final operational requirements of GaN devices (electrical operating mode, harsh environment, ...), reliability tests are required to determine the first order degradation signature, and its related mechanism to be modeled or solved. Reliability studies aim to make the technology pass the lifetime requirements. When passing a critical lifetime requirement (usually 10 years of operation), then the junction temperature requirement can be elevated towards higher limits. Hence thermal stresses are largely employed during life tests. Tests usually completed by GaN manufacturing companies according to widely accepted standardized stresses are listed below:

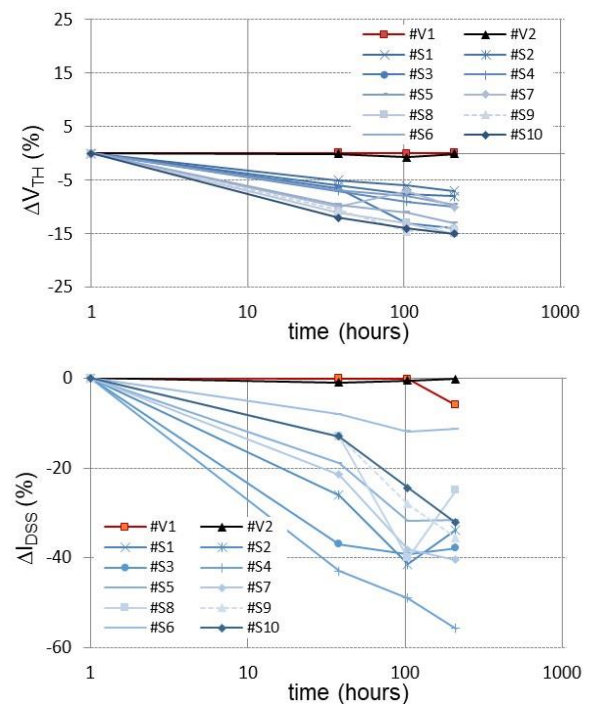


Fig. 2. Example of HTOL stress on a sample of ten 0.25x8x125μm² HEMT devices #S_i (the data for two virgin #V_j devices are also represented). Graphs report on the threshold voltage V_{TH} and on the saturation drain current I_{DSS} drifts during 210 hours of stress.

-DC life tests (DCLT): HTRB (high temperature reverse bias), HTOL (high temperature operating life, Fig. 2) and I_{DQ} - I_{GQ} (variations of drain or gate quiescent current at ambient temperature under class-AB operation) can be operated at different constant drain-source voltages (V_{DS}), or by step variation. Different parameters are tuned during the stress period (biasing drain current $I_{Dquiescent}$, saturation drain current I_{DSS} , threshold voltage V_{th} , leakage currents I_{G-leak} - I_{D-leak} , static transconductance g_m , drain and gate voltages). The stopping condition of the stress is usually given at 10% variation of $I_{Dquiescent}$, or according to a limitation of leakage current before destruction of the gate.

-RF life tests (RFLT): CW signals at various output power levels (compression) are convenient to capture time variation of the dynamic and static parameters over long time periods. Step stresses are used to assess the aptitude of the devices to sustain critical RF levels for rugged applications.

-Additive stresses can also be achieved under given ambient conditions (moisture, radiation, mechanical vibration & acceleration, etc...), but generally applies to packaged devices rather than on-wafer transistors.

Each DC life test is very time consuming, and several tests are required to evidence one degradation or acceleration parameter. RF tests are closer to the application context but more difficult to analyze because of possible conjugated effects. Scaling factors are then used based on the DC tests, but at the expense of a longer analysis period (if 1000 hrs per single test is performed, more than three DC tests and at least one RF test are required which corresponds to half a year if cumulated).

B. RF-Thermal experimental stress workbench

This workbench can be developed for specific application purposes and appropriate stress tests. For example, the robustness of a rugged low noise amplifier (LNA) versus jamming signals for radar applications is required to study the behavior of the device/circuit versus RF step stresses (different tests, recovering periods, removing charge procedures). RF stresses are one of the harshest tests as all the DC-thermal-RF swings make the puzzle more difficult with more parameters to simultaneously consider. More than ever, setting an appropriate experimental procedure to discriminate between some potentially correlated degrading parameters is required.

An evolving RF stress workbench with programmable thermal pattern of the oven was developed. It allows the tracking of static quiescent conditions of the devices under test and the dynamic powers at the input/output ports of the devices at RF stress frequencies between 0.01 GHz and 40 GHz. It also measures S-parameters by removing the RF-stress signal when switching to the S-parameters measurement mode. It is a major challenge during RF stresses to maintain constant operating conditions of all circuitry on the stress bench and to obtain feedback regarding the stability thereof from the device under test (DUT). Hence the reason for the close monitoring of the oven temperature and the ambient room temperature ($\pm 0.1^\circ\text{C}$ measurement accuracy). Very importantly, the configuration of our test bench incorporates four different channels, three of

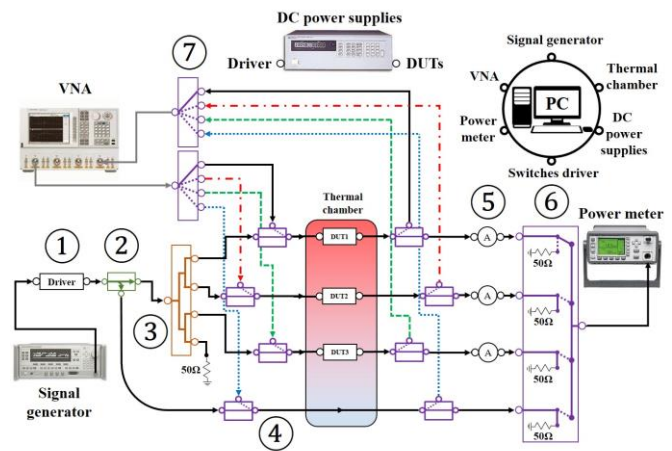


Fig. 3. Schematic diagram of the fully-automated workbench used for RF/thermal stress tests using step stresses or CW signals ranging from 0.1 GHz to 40 GHz. Thermal cycles rise and fall slopes are considered for temperature stabilization of the devices (from -40°C to $+150^\circ\text{C}$). A vector network analyser (VNA) collects S-parameter data with individual calibration set for each channel at intermediate times (very small variation of the calibration during hot/cold cycles and over a large period of use, less than 0.12dB insertion losses over two weeks). ① power amplifier, ② coupler, ③ four-way power divider, ④ SPDT switches, ⑤ attenuators, ⑥ SP4T 50Ω RF load terminations and ⑦ SP4T switches.

which are devoted to the DUTs, and a control channel which facilitates the analysis of potential drifts from the driver modules, that is, the signal generator and driver power amplifier shown in Fig.3. The stability of the calibration is verified at room temperature over 500 hours, and for thermal cycling conditions between -40°C and $+100^\circ\text{C}$ over one week (168 hours). The experimental setup features drifts below $\pm 0.05\text{ dB}$ (resp. $\pm 1^\circ$) at ambient room temperature, and below $\pm 0.04\text{ dB}$ (resp. $\pm 2^\circ$) for -40°C to $+100^\circ\text{C}$ thermal rectangular cycling, for the magnitude (resp. phase) of S-parameters. In the main stress paths, the total RF power fluctuations correspond to the drift of the 10 MHz to 50 GHz HP 83650B synthesized signal generator coupled with the 50 MHz to 50 GHz HP 8487A power sensor and to the Agilent E4418B power meter measurement uncertainties. The combined power drift at -40°C , $+25^\circ\text{C}$ and $+100^\circ\text{C}$ is respectively of $+0.01\text{ dB}$, $+0.03\text{ dB}$ and $\pm 0.02\text{ dB}$.

C. Illustration of RF-stresses at different RF compression levels of the DUT

CW RF stress tests are carried out for a given technology in the C- and X-bands. Fig. 4 presents an example of the variation of the drain current I_{DS} and output power P_{OUT} for a representative device under stress at three different output power compression points (1 dB, 3 dB and twice 5 dB). Between each RF-stress, a positive DC voltage of $V_{GS} = 1\text{ V}$ (shorted drain) can be applied to the DUTs to recover the initial electrical state for each device (due to a possible accumulation of charges during the stress). After each RF stress period (1 dB, 3 dB, 5 dB #A and 5 dB #B output power compression points), the drops of the drain-source current ΔI_{DS} are 3.9%, 5.6%, 5% and 3.4% respectively. The drops in output power ΔP_{OUT} are 10.4%, 13.5%, 10.5% and 7.2% respectively. It is obvious that the change in the static and dynamic plots are more pronounced

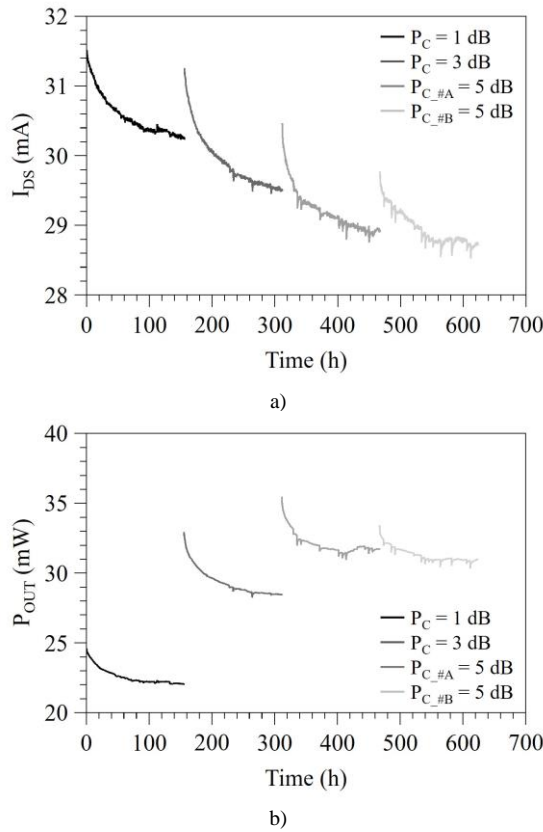


Fig. 4. C-Band CW RF stress impact on a $0.25 \times 2 \times 75 \mu m^2$ HEMT at chamber temperature of $+25^\circ C$. P_{OUT} versus time at 1 dB, 3 dB and 5 dB (#A and #B) output power compression points for quiescent point at $V_{DS} = 15$ V and $I_{DS} = 35$ mA (each stress is applied for 1 week, i.e. 156h for a cumulated 624h of RF stress). a) DC drain current and b) RF output power vs time

at elevated compression levels, and are certainly due to higher non-linear effects as will be discussed in paragraph IV.

Fig. 5 presents these variations in the power of the RF signal versus those of the DC drain current. A linear trend globally results from DC and RF variations and can be used to model the interdependence of the RF power with the carrier density in the 2DEG channel (i.e. static drain current I_{DS}). From the linear regression of the power versus DC drain current (red plots in Fig. 5), a model can be found using the stress level (in dB) as an acceleration factor of DC and RF degradation with time

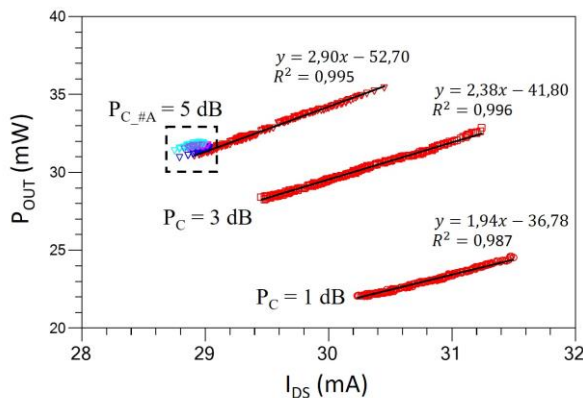


Fig. 5. Correlation between P_{OUT} and I_{DS} from Fig. 4 at 1 dB, 3 dB and 5 dB (#A) output power compression point. #B is not presented for improved clarity, due to the overlapping of the 5 dB #A and #B plots.

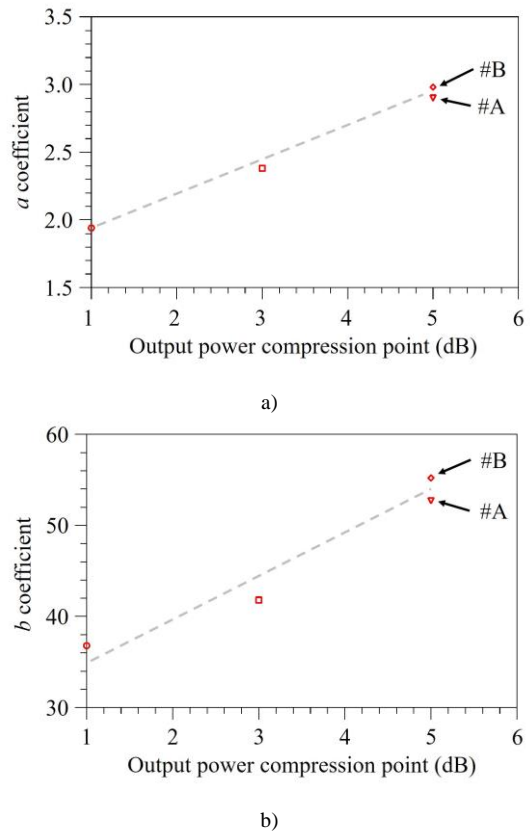


Fig. 6. Affine function coefficients ($P_{OUT} = a I_{DS} + b$) for the device under test from Fig. 5, at 1 dB, 3 dB and 5 dB (#A and #B) output power compression point. (a) and (b) shows the relation between the activated degradation mechanism number during the stress (red linear regressions from Fig. 5).

(Fig. 6). Specific behaviors at the end of the 5dB compression RF stress (dotted rectangular area in Fig. 5) also give interesting inputs about the kinetic of recoverable or permanent degradation effects (#A and #B), and related information can be found in [11].

This data is used together with other characterization and simulation tools presented in the next sections to complete the map for understanding the underlying fine mechanisms of the stress. Here, accumulation of positive charges under the gate change the intrinsic bias of the 2DEG and modulate the carriers density n_i (thus I_{DS}). The dynamic gain S_{21} evolves (dBS_{21}) and the $P_{1\text{dB}}$ compression point decreases as also revealed on the same sample of devices during X-band stresses [7]. From S-parameter measurements (illustrated in Fig. 7 at 5dB compression), the input impedances (or S_{11} reflection coefficient) of the tested devices remain stable over time at each compression level. Hence, it can be stated that the electrical elements between gate and source pads are kept unchanged (access resistances on gate R_G and source R_S , intrinsic resistance R_i , and gate-source capacitance C_{GS-i}). Thus, time evolution on S_{21} correlates with change of the dynamic transconductance gain g_m , or with change of the intrinsic potential applied to the capacitance C_{GS-i} (vertical stacking of charges at layers interfaces below the gate Schottky diode [10]). By using a fault tree method together with pertinent dedicated measurements or models, it is possible to guarantee the validity and the reliability of the interpretations.

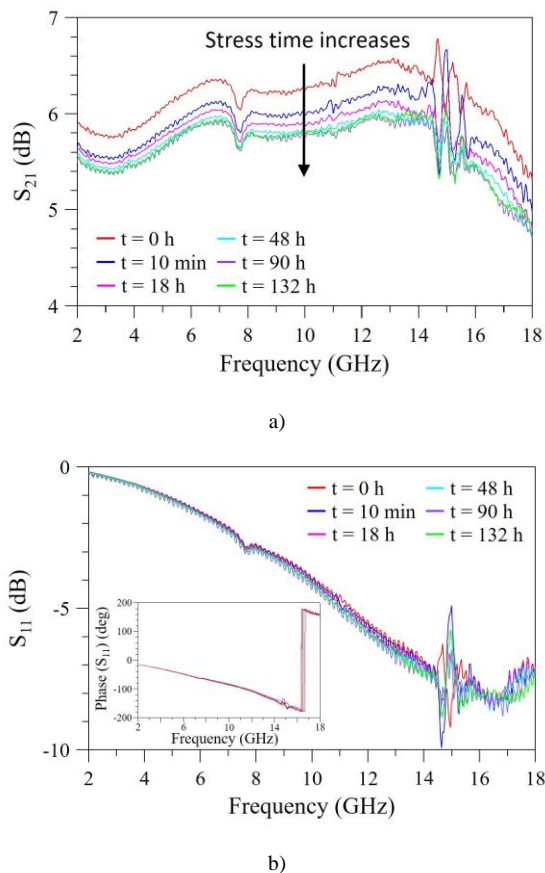


Fig. 7. S-parameter evolution during 132 hours of stress at 5dB output power compression point. a) changes are noticed of the magnitude of the transmission gain S_{21} , whereas b) the magnitude and the phase of the input reflexion coefficient S_{11} remains stable.

In addition to the three questions usually posed by industrial founders for a process qualification (what happens? when does it happen? where does it take place?), two more questions must be addressed (how and what do the defects reveal?). These last two questions usually need specific experimental workbenches available in academic laboratories. The next section shows some experimental setups used for failure analysis studies, the

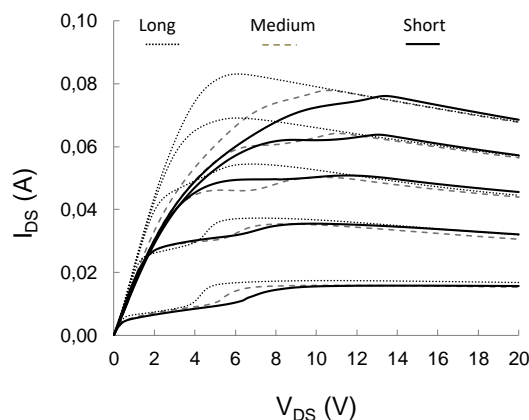


Fig. 8. Illustration of invasive DC-measurement on the output characteristics of a $0.25 \times 2 \times 50 \mu\text{m}^2$ HEMT (Measurement performed on an immature InAlN/GaN HEMT process). I-V characteristics are given for different acquisition time configurations (acquisition time per data point - Short=640μs / Medium=20ms / Long=320ms) using 4156C Keysight Signal Analyser.

objectives of which are to answer to the previous set of questions.

III. DIFFERENT CROSSED EXPERIMENTAL TECHNIQUES

GaN HEMTs are notably robust wide bandgap devices, but they are also sensitive to electrical charges, depending on local or global thermal states, on electrical fields and mechanical strains due to spontaneous and piezoelectrical charges at different interfaces of the layers. Related defects and resultant failure analysis can be revealed with experimental tools, directly by targeting the active area (destructive tools) or by deduction from external measurements (non-destructive tools).

A. Non-destructive techniques before/during/after stress

Experimental tools allowing electrical (transient or harmonic) characterizations are attractive because the device under test is not supposed to evolve during the characterization. Then consequent sets of data can be compared at different stress times for fine analysis or modelling (for the instruction of electrical model or that of TCAD model). However, the measurement is mainly extrinsic to the invoked zone where the failure mechanism takes place, and a rigorous procedure associated with the experimental setup is needed to lower the speculative aspects of the resulting outcomes. A very important consideration is that a non-destructive measurement technique does not necessarily mean non-invasive measurement. Test conditions may interact with some defects according to the setup of the workbench. Fig. 8 illustrates the sensitivity of a new generation InAlN/GaN HEMT device relative to the acquisition time instructed for a signal analyzer during so-called 'static' or 'DC' output I_{DS} - V_{DS} (and transfer I_{DS} - V_{GS}) characteristics.

When such variations occur in the output 'static' characteristics, then electrical models using short or medium

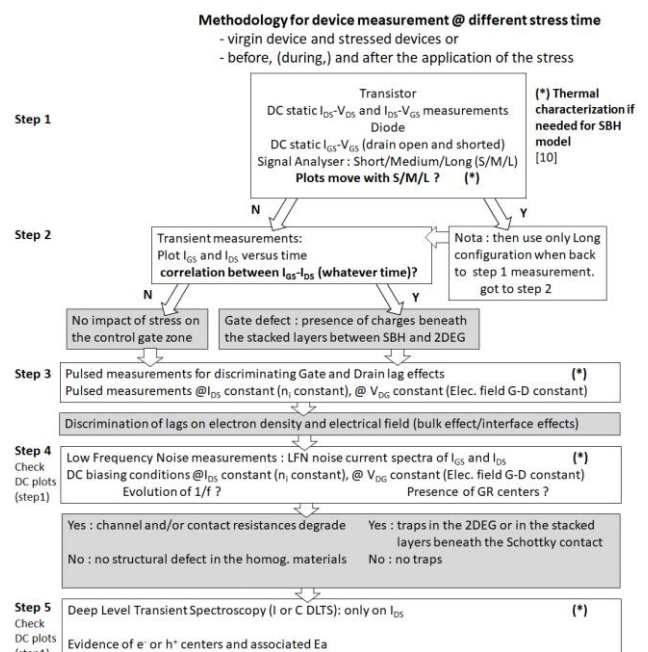


Fig. 9. Measurement methodology using transient and harmonic measurements to reveal defects in the HEMT. Comparison between initial/final measurements defines the location and the origin of the defects.

measurement configurations are erroneous due to those side effects which are considered as the manifestation of memory effects. Even during the measurement of S-parameters, frequency dispersion can appear at frequencies well below the starting frequency conditions (usually set at 40 MHz) [12]. In the case of DC or S-parameter variation according to measurement conditions, resultant models will be inappropriate for analysis before, during or after the application of a stress and hence inappropriate for circuit design.

The methodology used for each characterization before and after the application of the stress is depicted in Fig. 9 where the experimental setup complementarity is associated to the various sweep conditions (time, frequency or temperature). In this procedure, data from the stress file, that is, P_{out} , DC current and S-parameter versus time data, are analyzed together with the initial and final set of measurement data as proposed in Fig. 9. It is also possible to partition the stress campaign to have more intermediate results.

- DC measurements form the reference measurement to ensure the integrity of the electrical signatures of the DUTs during the procedure depicted in Fig. 9. If the characteristics of these DC measurements change, then the finer analysis between step 1 and step 5 provide nonsensical data and hence are non-valid (steps 2, 3 and 4).
- Transient measurements provide the first insight into short-, medium- and long-term memory effects or trap related effects. Moreover, the possible correlation between $I_{GS}(time)$ and $I_{DS}(time)$, as depicted in Fig. 10 a), provides first order information about the common nature of the defect charges under the gate [10]; this corresponds to step 2 of Fig. 9. This

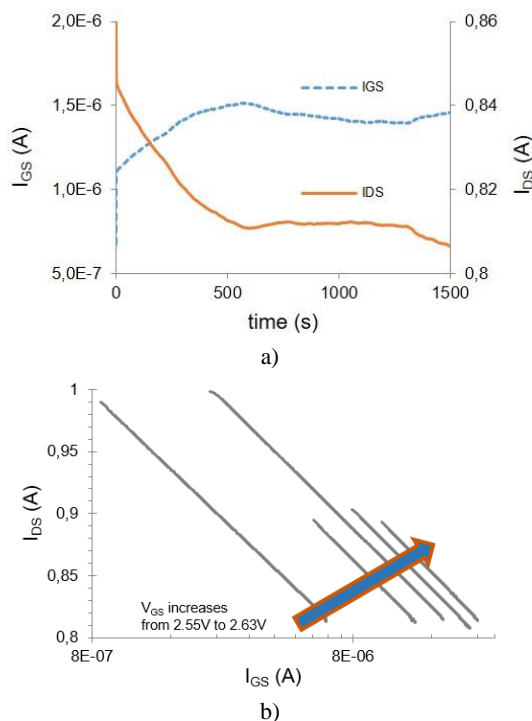


Fig. 10. DC leakage current I_{GS} and drain current I_{DS} variation for a 1 mm equivalent width GaN device. a) Evolution versus time over 1500 seconds for a given quiescent point $V_{GS}-V_{DS}$, and b) Napierian logarithmic correlation according to $I_{DS}=\ln(I_{GS})$ for different quiescent points on the overall transient screen.

information provides evidence of time-varying charges under the gate, the effect of which is to de-bias the intrinsic V_{GS-i} control voltage, resulting in a simultaneous affect to both I_{DS} and I_{GS} as depicted in Fig. 10 a) (a first order linear dependence for I_{DS} and an exponential law for I_{GS} , as stated by the Napierian logarithmic relationship from Fig. 10 b). A procedure is proposed in [13] for lag analysis on gate and drain currents using pulsed measurements as depicted in step 3 of Fig 9.

- Low Frequency Noise spectra (LFN) spectra (from 1 Hz to 1 MHz) are known to be very sensitive to the quality of the material and to the presence of defects on the path where the current flows (gate S_{IG} and drain S_{ID} noise current spectral densities). Measurements under different biasing conditions permit the identification of DC voltage or current sensitive traps (generation-recombination centers if present in the measured spectra) (step 4). The literature often illustrates that S_{ID} remains constant before and after the application of a stress, despite numerous GR centers distributed over the low frequency range. This means that defects are present, which may vary with bias, but are not necessarily impacted by stress. In contrast, S_{IG} is very sensitive to charge or trap evolutions and forms an excellent marker of defects under the Schottky command [13][14].
- Capacitance or current deep level transient spectroscopy (C- or I-DLTS) measurements are performed over a temperature range of 90 K to 450 K as depicted in step 5 of Fig 9. Activation energies and cross-sections of the traps are extracted and compared with the GR centers from LFN measurements in step 4 [15].

Fig. 11 shows plots of the measured low frequency noise current spectral density S_{IG} on the gate, with the extracted contributors, that is, 1/f flicker noise, Lorentzian noise from

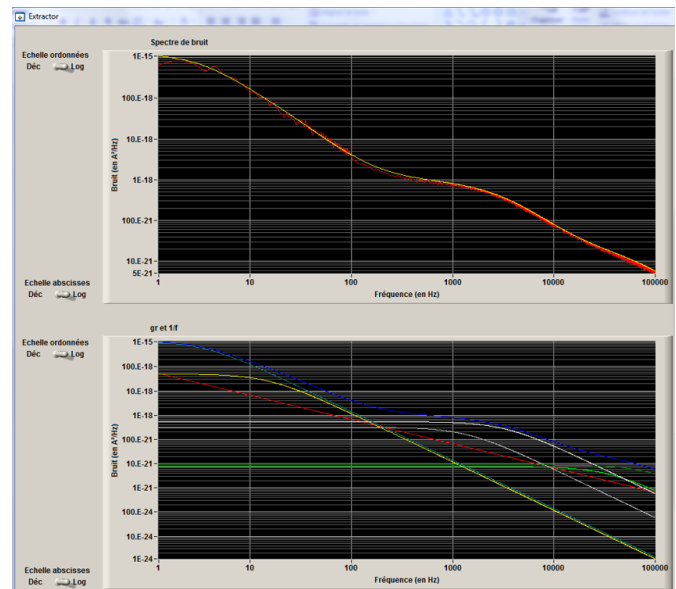


Fig. 11. Low frequency noise measurement (red) and resulting model (yellow) on gate current spectral density versus frequency (upper screen), with automatic extraction of noise contributors (lower screen). Here six different lorentzians (four generation-recombination and two RTN contributors) and 1/f flicker noise are shown and used to compose the blue plot model (yellow in the upper screen). Screenshot from proprietary software; for distinction of colors, please refer to the electronic version.

generation-recombination centers (GR) or random telegraph noise (RTN). RTN contributors are extracted by performing transient measurements and by using a routine for corner frequency and current variations shown in Fig. 12. The contribution of RTN can be plotted in the frequency domain by using equation (1) and compared to LFN spectra as illustrated in Fig. 11. Dedicated software developed in the laboratory allows the extraction of noise contributors from LFN spectra. The GR centers are then tracked and plotted versus biasing or temperature. This facilitates the extraction of activation energies [15], and the identification of the related bond-vacancy or other activation mechanism from comparison with the literature, or for example, by cross experimenting with energy-dispersive X-ray (EDX) spectroscopy or with Raman spectroscopy analysis. The same procedure was developed for the noise spectra on the drain current, under different constant voltage V_{DG} , V_{DS} , V_{GS} biasing conditions to appreciate the first order parametric law versus the electrical field, or versus the carrier density [13].

$$S(f) = \frac{2(\Delta I)^2 \bar{\tau}}{4 + (2\pi f \bar{\tau})^2} \text{ with } \frac{1}{\bar{\tau}} = \frac{1}{\tau_e} + \frac{1}{\tau_c} \quad (1)$$

τ_e and τ_c are related to the lower and higher states of the noise level respectively. Many levels are accounted for, as illustrated in Fig. 12, in the statistic extraction of random telegraph signals.

Additional characterization tools, which are not identified in Fig. 9, have successfully been used to identify and characterize defects in the devices under test. Examples of such tools are: photo emission microscopy (EMMI), the optical beam induced resistance change (OBIRCH) technique [16], electroluminescence, other athermal A-DCTS techniques [17] and capacitance-voltage (C-V) measurements. All these tools provide key complementary characterization information.

B. Destructive techniques before and after stress

Non-destructive techniques can also be considered as speculative because of the indirect proof given of a failure mechanism, especially when different defect mechanisms are

encountered. Destructive techniques focus on the active part of the defect (according to the difficulty in finding out the related location). If the manifestation of defects can be proved by direct location of structural/chemical degradation in a stressed device (compared to a virgin device), then the following question arises from such an approach: does this defect play a role in the electrical signature of the device? A statistical approach would strengthen the conclusions generated from these studies, but without doubt, it will prove difficult to check intermediate steps during stress periods which would imply many (homogeneous) samples for each stress, removing few devices at a given moment during the stress. Subsequently the correlation of studies as proposed in Fig. 1 reduces the risk of speculative answers by the cross analysis of independent results.

Very sensitive characterization tools such as high-angle annular dark-field scanning transmission electron microscopy (HAADF STEM) with atomic number contrast in the stacked layers, transmission electron microscopy (TEM) lamella after gate foot removing, or EDX spectroscopy analysis have been used in [18] with TCAD models and electrical measurements to differentiate the origins of defects responsible of various failure signatures.

IV. MODELS FOR FAILURE ANALYSIS

It is possible, using large signal electrical measurements, to develop non-linear models of a device and the availability of such a model with its associated failure signatures is useful for circuit design [18]. The design of a circuit at the initial t_0 and then considering parametric shifts at the final t_{stress} may assist the designer in the optimization of circuit topology.

In this case, TCAD models (using Sentaurus-Synopsys) are more relevant since the paper deals with failure analysis. 2D simulations of the active device facilitate the physical modeling of degradation mechanisms which enable the understanding of III-N HEMT failure modes. The specification of physical parameters in a given region of the model provides useful feedback on experimental results.

The effects of charges and traps in terms of nature, location, energy level, density, section, (bulk, interface, under the gated or ungated zones G-S and G-D) can be evaluated on the output I_{DS} - V_{DS} and transfer characteristics I_{DS} - V_{GS} (G_m - V_{GS}) [19], and on leakage currents I_{GS} - V_{GS} (diode and transistor mode).

After an exhaustive study regarding the manner in which the defects are specified, as well as the impact of donors or acceptors in the GaN bulk and at the different interfaces of the device, one can dispose of a large variety of parameters, each associated to a failure signature. Then, referring to the experimental plots, it is possible to tune such a TCAD model to match the measurement in a realistic way.

Donor-like centers in the bulk of the GaN layer account for magnitude variations in I_{GS} - V_{GS} as revealed by some HTRB or HTOL stresses. It is probable that, for a fixed activation energy of the donor-like centers, only the concentration increases with the application of the stress, as illustrated in Fig. 13 a) where the donor-like center is located at the SiN/GaN cap layer interface. The rapid increase in the leakage current from part of this inversion voltage, featuring a plateau, is reported in many

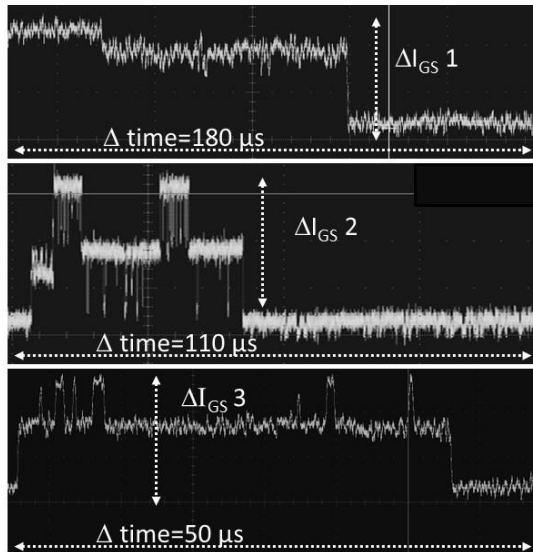


Fig. 12. Random telegraph noise transient measurements can be modeled and their contribution can be distinguished from GR Lorentzian curves in Fig. 11.

papers [20][21], and is also applicable to GaN-based LEDs [22]. Furthermore, Fig. 13 b) illustrates how the inversion voltage shifts, which are mainly due to various donor concentrations, and for activation energies situated at 0.3 eV below the conduction band E_C , in transistor mode (no variation of V_{th} versus n_D is revealed for ‘deep centers’ as reported for $E_D=0.5$ eV below E_C). The closer the activation energy is to the conduction band, the more pronounced is the variation shift of the inversion voltage. Depending on the epitaxial and passivation process, the simulation can fit to account for specific electrical signatures.

Other methods of electrical modelling of HEMT devices can be used to account for fine charge effects, or the influence of defects in the active zones or in the command definition. The accuracy of such a model, and its aptitude to translate the physical behaviour when embedded in a circuit context, is mandatory to enable power devices to work close to their maximum safe operating conditions. Another point is to provide

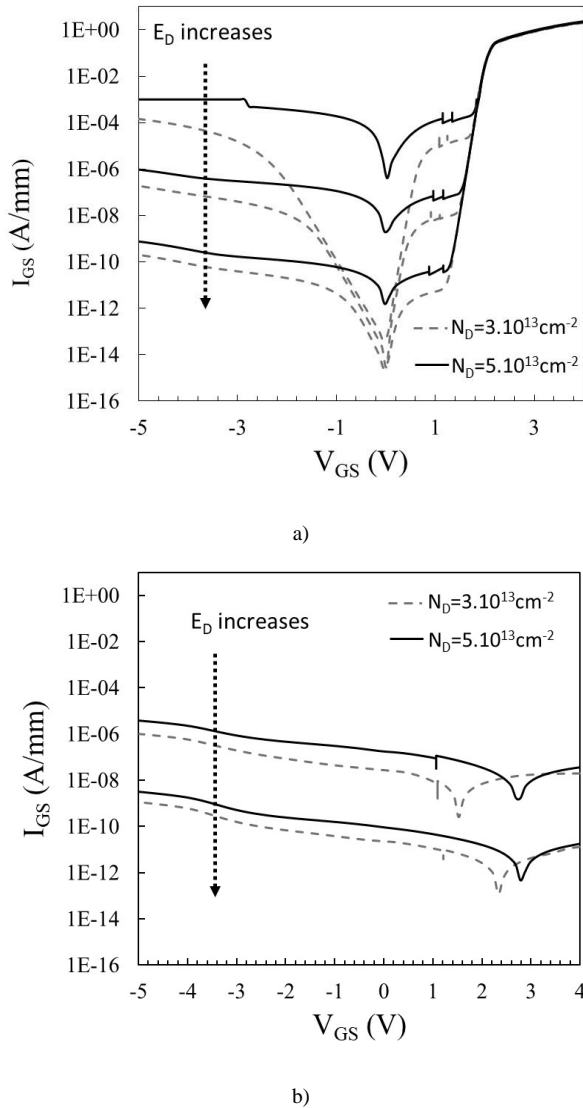


Fig. 13. Simulated leakage I_{GS} - V_{GS} characteristic ($V_{DS}=0$ V for figure a, and $V_{DS}=8$ V for figure b), versus different donor activation energies and concentrations. Energies E_D are situated at (0.1eV figure a), 0.3 eV and 0.5 eV below the conduction band, with donor concentration n_D at $3.10^{13} \text{ cm}^{-2}$ and $5.10^{13} \text{ cm}^{-2}$.

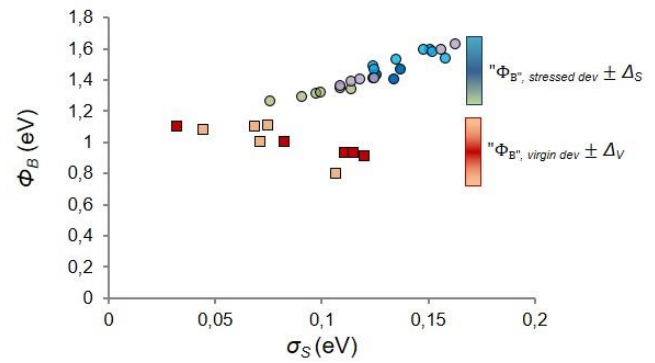


Fig. 14. Variations of $\overline{\Phi_{Bx}}$ versus σ_{Sx} at temperatures ranging from 200 K-400 K), for various gate current ranges (2 decades sliding gate current window), for 2 virgin samples (squares) and 4 stressed samples (circles).

confidence to the circuit designer concerning the mean time to failure, and so to integrate models of the device at t_0 (initial performances) and t_{max} when dynamic or static criteria are degraded by, for example, 10%. Since the command, or at least the vertical stack under the command, seems to play a crucial role in the degradation processes of I_{DS} and P_{OUT} , the specific model of the Schottky barrier height (SBH) must be accurately constructed in the electrical models. From the literature, the extraction of the SBH value is usually over-evaluated with ϕ_B ranging between 1.1eV and 1.6eV, while the theory stipulates an approximate value of 0.9eV for ϕ_B . We have developed a method for the accurate extraction of the mean SBH, over a wide range of leakage currents and temperatures [19][23]. Then, after processing the mean SBH for different inhomogeneity of the barrier, it is possible to extract the ideal SBH on the $\sigma_s=0$ eV intercept point (that is, with no inhomogeneity or defect). Using Fig. 14, two virgin and four stressed devices were processed, all featuring an ideal SBH around 1 eV at zero dispersion σ . The impact of the stress is noticeable, with virgin devices featuring a lower SBH and with stressed devices featuring a higher SBH. Thus, the need of stability for the gated control zone, and its correlation with the degradation of the devices, is clearly highlighted.

V. GLOBAL OVERVIEW CONCERNING FAILURE ANALYSIS RESULTS FROM PREVIOUS STUDIES ON GAN HEMTs

Utilizing the proposed set of experimental and simulation tools, we can reduce the number of speculative assumptions regarding those possibly involved mechanisms from a given file of stress. The detection and the location of charges at different interfaces under the gate and between the gate-source and gate-drain regions, the possible transient correlation between gate and drain currents related to time-varying charges under the gate, and the analysis of the gate leakage current behaviors versus temperature are some of the outcomes from such previous work. Since one of the dominant failure modes of GaN HEMT devices relates to a gradual decrease in RF output power (wear-out), which is generally correlated with the (recoverable) decrease in the drain current (current collapse), studies have been focused on the impact of RF power stresses. The role of RF-activated traps and charges have been identified on the degradation mechanism for different compression levels.

Moreover, the leakage current is an efficient marker of the degradation mechanisms [24], and a direct link can be established between the current level I_{GS} and the MTTF as shown by [25]. Hence, the study thereof can be considered as the most relevant part of nitride technology improvement. Using some of the studies summed up in this paper, we can discriminate between defects in the channel (usually not stress-dependent) and defects activated by stress in the outer zones of the main electron flow (from source to drain), featuring recoverable or permanent effects. These techniques have made it possible to improve different academic and industrial GaN processes.

VI. CONCLUSION

The optimization of a GaN technological process involves the understanding and the mastering of failure mechanisms, while still maintaining a roadmap towards increased frequency of operation and power added efficiency. Failure analysis for RF stresses are among the more difficult to achieve as many parameters are involved in the various RF and DC electrical signatures before and after the application of a stress. A set of DC/thermal/RF stress tests are usually needed for the identification of such degradation processes, which require long study times. In this paper a set of non-destructive measurement techniques are identified that can be confirmed with TCAD simulations to secure the failure analysis as presented in Fig. 1. It is then possible to identify root physical degradation defects involved in many different (RF or DC) electrical signatures from a single RF life test. Notably, this methodology does not allow the extraction of activation energies needed to get the mean time to failure. However, it can easily be achieved if used with three different temperature life tests.

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