Experimental and microscopic analysis of 600V GaN-GIT under the short-circuit aging tests

J-Z. Fu, F. Fouquet, M. Kadi
Normandie UNIROUEN,
ESIGELEC, IRSEEM
76000 Rouen, France

F. Cuvilly, P. Dherbécourt
Université de Rouen-Normandie–GPM UMR CNRS 6634
Avenue de l'université B.P 12
76801 Saint Etienne du Rouvray, France

***Abstract*—this paper presents experimental short-circuit aging tests of a 600V GaN (Gallium nitrite) GIT (Gate Injection Transistor). The short circuit aging tests effect under the drain voltage equal to 35V and the three short-circuit durations (1ms, 2ms and 4ms) are investigated. The evolution of the electrical characterizations is well shown in this paper. A microscopic analysis, related the degradation mechanism, is proposed in the paper.**

Keywords—GaN GIT, short-circuit test, energy, electrical charactrizations, microscopic analysis

I. INTRODUCTION

As one of the most promising wide band-gap (WBG) semiconductor technology, the GaN (Gallium nitride) HEMTs (High Electrons Mobility Transistors) are expected to be promising devices for high frequency, high power density converter [1]-[2] with the advantages of high withstand temperature, high breakdown voltage and high-speed commutation. As known that most of the GaN HEMTs have a normally-on (depletion) mode with a negative Vth (Gate threshold voltage), normally-off (enhancement) mode are required for the power electronics applications in order to reduce the circuit complexity and prevent the destruction due to short circuit when the failure of the gate signal occurs. In [3], the authors have resumed the different technologies to achieve the normally-off mode for the recent commercial GaN-based normally-off transistors.

In order to widely use GaN-based transistors for the construction of power converters, several operating conditions must be satisfied, especially the short-circuit event, which is an operational and critical mode that must be solved. Transistors must be able to withstand the short-circuit event during few microseconds (typically 10 µs) before the failure of the gate signal is detected and cleared [4]. Several works in the literature are dedicated to the study of the robustness of the GaN-based under the high voltage short-circuit event. The author in [5] has reported that a 200V-rated commercially GaN-based transistor could only withstand 2 µs of short-circuit at 50% of the nominal voltage. In [6], 600V-rated GaN-based transistors form GaN Systems Company showed a very large disparity in the short-circuit test: while a few devices could withstand 500 µs, others failed after just a few hundred nanoseconds. The robustness test induces usually the catastrophic failure, and once the failure occurs, the device is destroyed and then non characteristic information can be obtained to understand the failure mechanism.

In order to reveal the degradation trend of the components after short-circuit stress, repetitive and non-destructive short-circuit tests under a relatively low drain voltage and a long pulse duration are proposed; which would help us to obtain gradual and partial failure; In this work, we have focused on the degradation mode during short-circuit repetitive test. This approach, already applied for the study of SiC MOSFET, as in [8] in which a commercial 1.2KV SiC MOSFET has been stressed by a repetitive short-circuit test under a 50V drain voltage, a 20V gate voltage (the maximal value) and the pulse duration varies form 100µs to 1000µs, and has demonstrated a gate oxide degradation by short-circuit aging test, while the drain voltage is 50V and the pulse duration varies from 100µs to 1000µs. In this paper, experimental results of repetitive short-circuit degradation for a 600V GaN GIT are investigated. After this introduction, we focus in Section II on the experimental bench and repetitive stress conditions. Section III addresses the evolutions of electrical parameters during the repetitive short-circuits. Section IV present a microscopic analysis which is related to the degradation mechanism proposed by the evolution of the electrical parameters.

II. EXPERIMENTAL SETUP DESCRIPTION

A. Experimental device

The device under test (DUT) is a 600V GaN-based transistor which uses a commercial technology as a non-insulated gate-

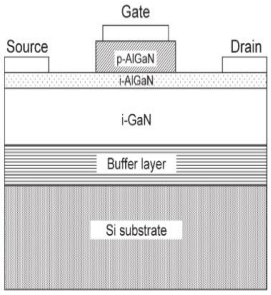

Figure 1. Cross section of the GIT structure [9]

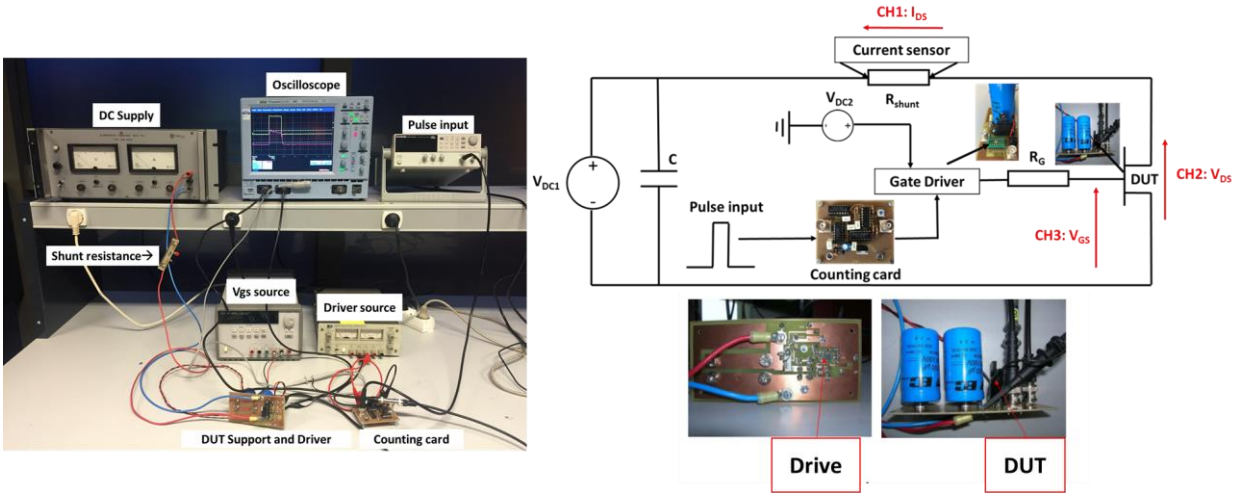

Figure 2. The set-up for short-circuit test

-structure named Gate Injection Transistor (GIT) with TO-220 packaging, provided by Panasonic. As in [9], a p-doped AlGaN layer is deposited under the gate that lifts up the potential of the triangular well at the AlGaN/GaN interface, which converts a normally-on operation to normally-off. The fig. 1 shows the cross section of this device. This conception makes the electrons accumulated by the injected holes to achieve a conductivity modulation which results in a significant increase of the drain current and keeps the gate current low.

B. Experimental bench

Fig. 2 illustrates the test bench schematic and picture used for the short-circuit testing of DUT. During the short-circuit test, the drain is directly connected to the DC supply and the gate is connected to a matched driver with a resistance. The DUT is turned on with the short-circuit conditions by applying a +3.7V gate-source voltage pulse (this value is sufficient to maintain the DUT at the on-state during short-circuit operation) which is a bit lower than the maximal value of 4.5V, then it is turned off by applying a negative voltage to gate. The drain current Ids is then measured by using a 10mΩ shunt and a high side current sensor which produce a 50mV/A output voltage, then this voltage is recorded with an oscilloscope. The counting card could achieve cycles of 4096 pulses. The pulse period is fixed by T=1s between two successive pulses which is defined by the pulse generator and the pulse duration can be adjusted by counting card as needed.

C. Experimental conditions

The stress conditions are defined using the results of the DUT behavior under short-circuit test for different drain voltages and pulse durations [10]. These stress conditions of the repetitive short-circuit aging test used in this paper are summarized in the Tab. I. PAC#1, PAC#2 and PAC#3 have been stressed by the different energies. The parameter which allows to control this energy is in our case the pulse duration. The energy is calculated by the formula (1):

$$Esc = Vds \times \int_0^{Tsc} Id(t)\,dt = Vds \times \overline{Id} \times Tsc \qquad (1)$$

E_{sc}: The dissipated energy during the short-circuit

T_{sc}: The pulse duration

$\overline{Id}$: The average drain current

We have launched almost 40 cycles (1 cycle = 4096 pulses) in total. The electric characterizations, I_{DS}-V_{DS} (I_{DSSAT}), R_{DSON} (on state drain-to-source resistance), V_{TH} (gate threshold voltage), I_{DSS} (Leakage drain current) and I_{GSS} (Leakage gate current), are regularly measured at 25°C by our pulsed I-V measurement test bench . The measurement conditions provided by the datasheet are resumed in Tab. II

TABLE I. EXPERIMTAL CONDITIONS FOR 2 DEVICES

DUT	PAC#1	PAC#2	PAC#2/PAC#3
V_{DS} (V)	35	35	35
The pulse duration	1ms	2ms	4ms
Dissipated energy	147.6 mJ/mm^2	232.75 mJ/mm^2	420 mJ/mm^2
Numbers of cycles	190,000	150,000	8,000/33,000
The state	Degrade	Degrade	Abnormal/Failure

TABLE II. THE MEASUREMENT CONDITIONS FOR ELECTRICAL PARAMETERS

Electrical parameters	Measurement condition
R_{DSON}	V_{GS}=3.7V, I_{DS}=8A
I_{DSSAT}	V_{DS}=5V, V_{GS}=2.5V
V_{TH}	V_{DS}=10V, I_{DS}=2.1mA
I_{DSS}	V_{DS}=600V, V_{GS}=0V
I_{GSS}	V_{GS}=4.5V, V_{DS}=0V

III. EXPERIMENTAL RESULT

A. *Evolution of I-V characteristics*

The output characterization I_{DS} versus V_{DS} for PAC#3 during the repetitive short-circuit test (before the failure) is illustrated in fig. 3. The PAC#3 component has been sustained for 33K short-circuit cycles at T_{SC}=4ms. A regular and large drop can be observed in I_{DS} for both linear and saturate regions. The decrease in linear regions represents an increase of R_{DSON}. These two correlated phenomena, indicating a reduction of device conductivity (The reduction of I_{DSSAT}), can be induced by the degradation of the source metallization layer. Fig. 4 presents the evolution of input characterization I_{DS} versus V_{GS}. The regular drop in linear region could be also clearly observed. The parameter V_{TH} extracted by this curve will be presented in Section III-C.

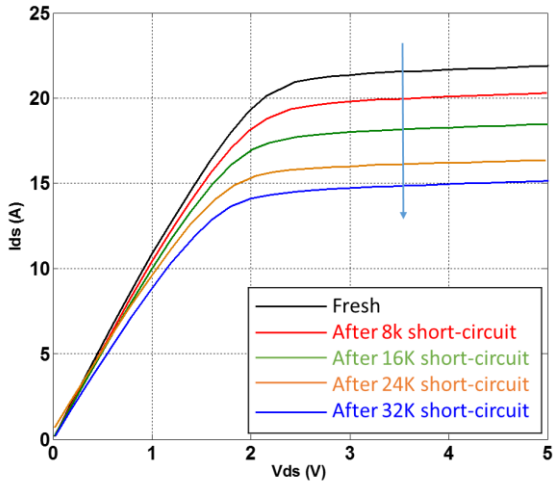

Figure 3. Evolution of I_{DS}-V_{DS} at V_{GS}=2.5V and T_{SC}=4ms for PAC#3

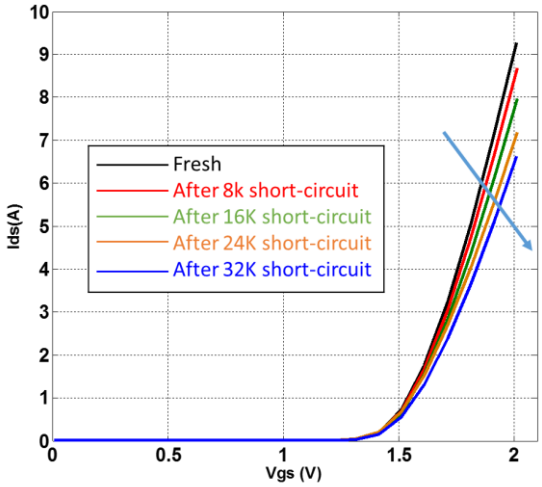

Figure 4. Evolution of I_{DS}-V_{GS} at V_{DS}=10V and T_{SC}=4ms for PAC#3

B. *Short-circuit behaviours*

After 32K short-circuit cycles at T_{SC}=4ms, the short-circuit drain current of PAC#3 present a significate reduce, as shown in fig. 5. Since the last short-circuit current was measured at the end of repetitive tests before failure occurs, we speculate that a part of this reduction is due to the recoverable thermal effect, another is permanent degradation.

After 8K short-circuit cycles at T_{SC}=4ms, an unstable behavior of PAC#2 is observed. Fig. 6 presents one of PAC#2's short-circuit currents under this kind of behavior. For this case, I_{DS} sudden decreases completely to zero at 1ms, which turns DUT at off-state. By measuring V_{GS} at the same time, we can observe that the driver cannot any longer modulate the voltage supplied by V_{DC2} (see Fig. 1). The other cases are similar, only the time to turn off has changed. At the turn-off region, a significate drain leakage current can be measured.

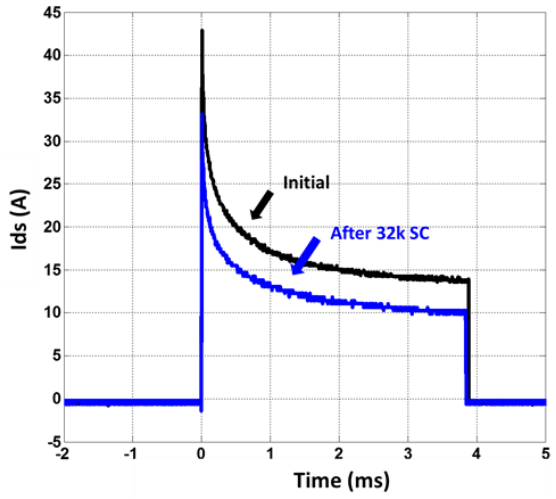

Figure 5. Short-circuit waveforms for PAC#3

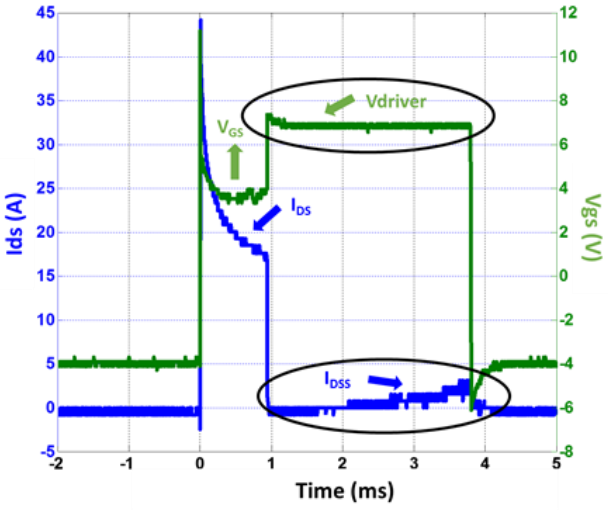

Figure 6. Short-circuit waveforms for PAC#2

To better understand this behavior, we have done several investigations:

1. The characterization of PAC#2 remain normal. No catastrophic failure occurs.
2. The tests for others fresh components can eliminate the driver's possible failure.
3. The short-circuit behavior of PAC#2 becomes normal if the pulse duration reduces.
4. When the repetitive short-circuit tests at T_{SC}=4ms start running, the unstable behavior of PAC#2 will not appear immediately. After a few pulses, the behavior happens which might be due to the reached high temperature.

In this behavior, due to a temporary failure occurred between gate and source at high temperature (open-circuit), the driver cannot any more deliver a constant current (10mA), which induces the equilibrium state between V_{GS}, V_{driver} and V_{DC2}. This kind behavior allows switching off the drain current and allows protecting the device from destruction between drain and source. The similar behavior could be also observed for the SiC BJT under the robustness short-circuit test [11], which is treated as a self-protection failure.

C. *Evolution of electrical parameters*

Fig. 7 presents the evolution of the principal parameters versus numbers of short-circuit pulses. The first parameter we observed is the R_{DSON} (see fig. 7(a)) measured at 25°C by extracting the I_{DS}-V_{DS} output characteristic. We observed a gradual increase in R_{DSON} during the repetitive short-circuit aging test for all components. It recorded a raise of about 9.5% for PAC#1 with T_{SC}=1ms after 190K cycles, about 14.5% for PAC#2 with T_{SC}=2ms after 150K cycles and about 20.7% for PAC#3 with T_{SC}=4ms after 32K cycles. This evolution results in a significant degradation, which might locate either at the-

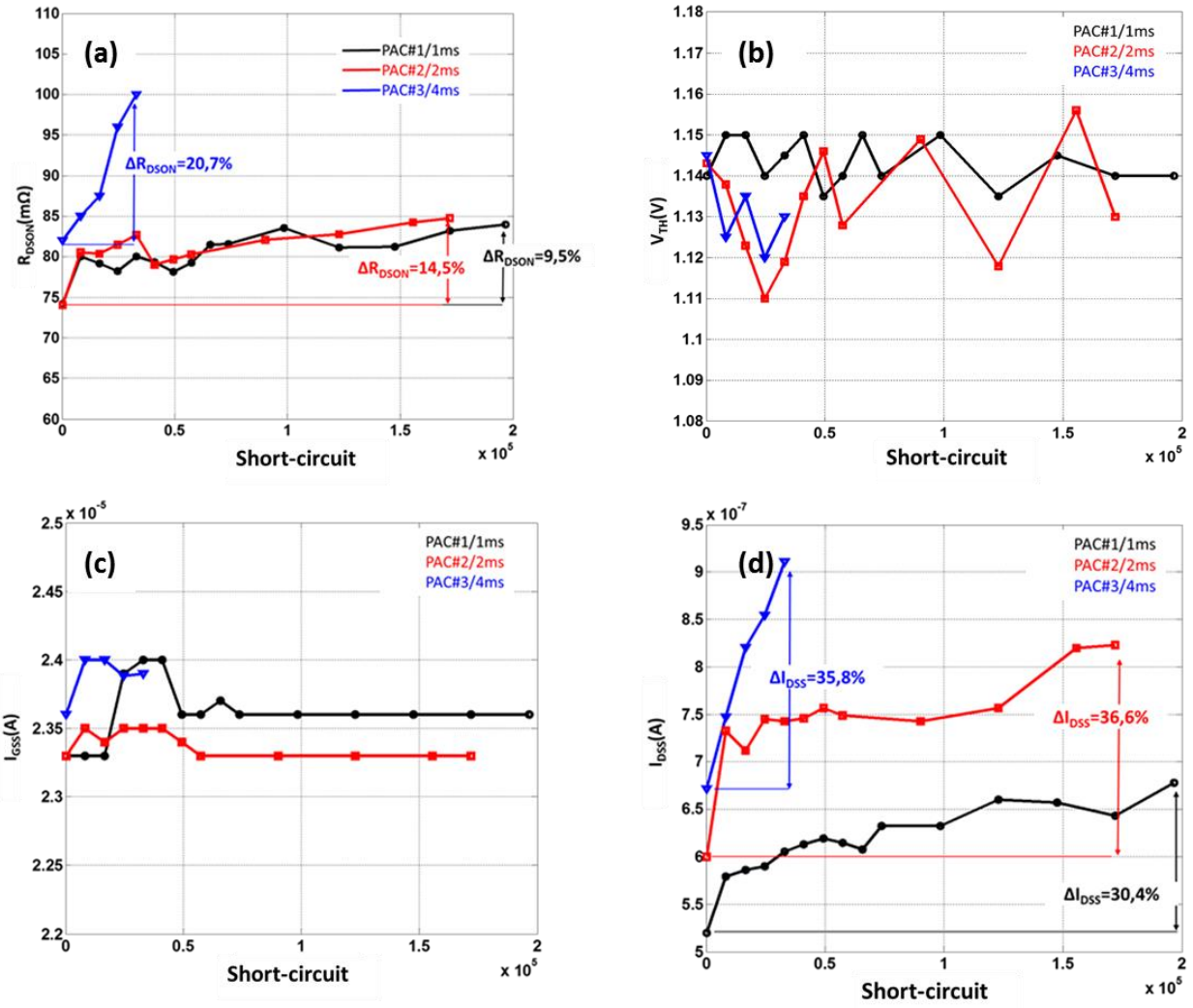

Figure. 7 Evolution of (a) R_{DSON}, (b) V_{TH} (c) I_{GSS} and (d) I_{DSS} versus numbers of short-circuit for PAC#1 (T_{SC}=1ms), PAC#2 (T_{SC}=2ms) and PAC#3 (T_{SC}=4ms)

-level of the bonding wires, or at the level of the source metallization. Similar results were observed on silicon components [12] where the increase in R_{DSON} was accompanied by a significant degradation of the metallization due to the reconstitution of Aluminum during the aging test. From the figure, we can conclude form this evolution that more dissipated energy per pulse is applied to the component, more significant degradation on R_{DSON} during the repetitive test.

By extracting the I_{DS}-V_{GS} transfer characteristic, the evolution of V_{TH}, as a function of the short-circuit numbers for the three components, is presented on fig. 7(b). According to the curve, no significant and regular variation is recorded during aging tests for all the three components. However, the V_{TH} evolution has a stable situation that the maximum variation is less than 4%, which is unlike the repetitive short-circuit test for the SiC MOSFET. According to [8], the V_{TH} evolution of the SiC MOSFET has progressively and significantly increased during similar aging test due to the oxide degradation. Anyway, similar variation as ours is observed in [13] for the GaN-GIT during the repetitive high-voltage short-circuit test until the failure occurs. So we could suppose that the GaN-GIT offer a fairly stable situation near the gate, especially that the p-GaN layer seem remain non-degraded state during this type of accelerated aging test. To better understand the gate-side state and reinforce the hypothesis of non-degradation near the gate during the repetitive short-circuit aging test, the evolution of the I_{GSS} is shown in fig. 7(c). As illustrated in this curve, I_{GSS} for the three components also shows a stable state with a variation less than 3%. However, the value of I_{GSS} remains quite high (the order of µA) compared to SiC MOSFET (the order of pA) [7], which is due to the hole injection effect by applying a positive gate voltage.

Fig. 7(d) shows the evolution of I_{DSS} as a function of the short-circuit numbers for the three components. For the PAC#1, I_{DSS} increases gradually until it reaches an increase of about 30% after 190K cycles. An increase of about 36% is observed on the PAC#2 after 150K cycles. The evolution of I_{DSS} for the PAC#3 shows an increase of about 35% after only 32K cycles. Among the evolution of all the electrical parameters, we note that I_{DSS} is an aging indicator which is most sensitive. Similar results are found in [14] concerning the experimental study of a 650V normally-off GaN-based transistor of ‘‘GaN Systems’’, the increase in I_{DSS} is probably related to the delamination of the solder layer which leads to a lower thermal conductivity.

IV. Microscopic analysis

The accelerated repetitive short-circuit aging test performed on the GaN-GIT has shown an increase of R_{DSON} which is probably due to the degradation at the level of the source metallization. Therefore, we assume legitimately that the defect could be found in the metal layer of the source-side. In order to confirm this hypothesis, the microscopic analysis is taken into account. For the microscopic analysis, the GaN-GIT with the packaging TO-220 has been uncapped according to the protocol of the laser ablation then of the chemical attack with the nitride

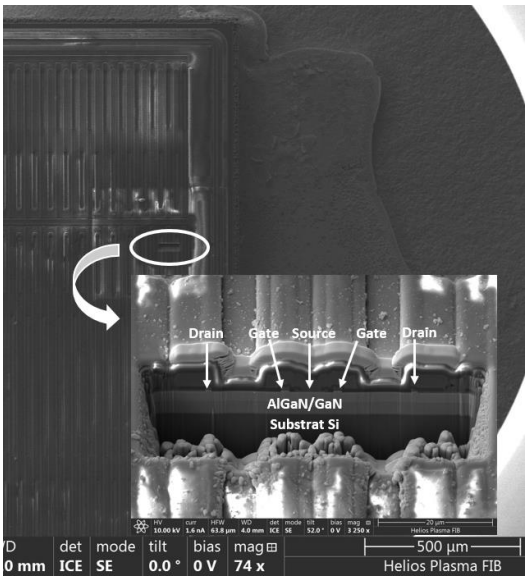

Figure 8. SEM cross section at the element cell by the FIB.

-acid. The observation by photoemission has been executed to locate the defect cell in the active surface of the puce. Once the defect was localized and for a finer analysis, the microscopic observation in the cross section of an elementary cell between the fresh component and the degrade component has been realized by the Thermo Fisher Helios G4 PFIB which combines the new PFIB 2.0 column (Plasma Focused Ion Beam) and the monochromatic Elstar™ SEM (Scanning Electron Microscope) column to deliver the most advanced focused ion- and electron beam performance, as shown in fig. 8.

In order to identify the defect, we focused in the gate-source region of the fresh component and the degrade component (PAC#2), as shown in fig. 9. We could observe for the fresh one (see fig. 9(a)), between the two stud p-GaN, a metal layer above the AlGaN layer achieves the ohmic contact for the source with the metal d’Aluminium. This metal layer for the fresh one show a uniform rectangle. But at the degrade one, serval cavities are presented in the metal layer, as shown in fig. 9(b). Thus, we could do the hypothesis that the degradation of the source metal layer is responsible for the increase of R_{DSON} during the repetitive short-circuit aging test

V. Conclusion

In this paper, we proposed a repetitive short-circuit aging test with a drain voltage equal to 35V and pulse duration variant from 1ms to 4ms for the GaN-GITs. Unlike the high drain voltage single pulse, which is used for the robustness analysis, our tests tend to behave the degradation trend of the component. During the aging tests for PAC#1 (1ms), PAC#2 (2ms and 4ms), and PAC#3 (4ms), R_{DSON} and I_{DSS} are the obvious indicators of the reliability of the components. Moreover, the greater energy-

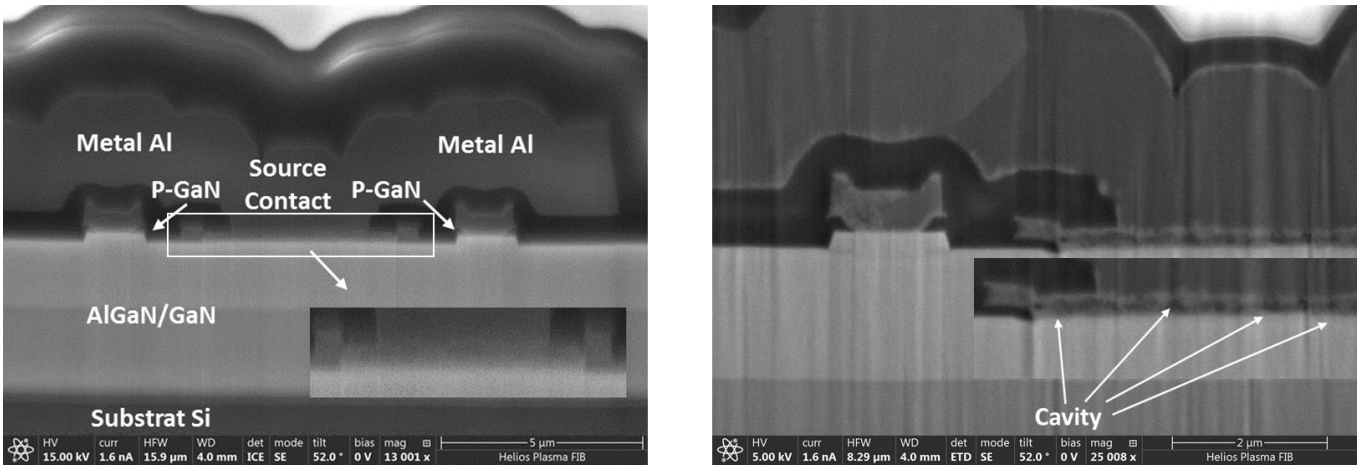

Figure 9. The cross section of the gate-source region for (a) the fresh component and (b) the degrade one

-per pulse is applied in the test, the more significant change could be found in the indicators. From the observed evolution, the change on I_{GSS} and V_{TH} is negligible, which shows probably a fairly stable gate performance during the aging test. The temporary open-circuit failure between gate and source is observed during the 4ms tests for PAC#2, which is due to numbers of short-circuit events. At the end, the microscopic analysis in the cross section of the chosen element cell has well presented the degradation at the level of the source metal layer, which is supposed to be a reason for the R_{DSON} increase during the aging test. In addition, the aging of the wire bonding is not presented in this paper as a factor that also induces the increase in R_{DSON}. The analysis by X-ray tomography in the DUT without opening the package will be concerned during the aging in the next study. Further study with higher voltage (until the nominal condition) but equivalent dissipated energy will be taken into account in order to identify the degradation mode related to the energy. In addition, the temperature evaluation induced by the self-heating during the aging test will be concerned by the simulation of the physical model in order to better understand and confirm the degradation mechanism.

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