An Improved SPICE Model for the Study of Electro-thermal Static Behavior for two New Generations of SiC MOSFET

W Jouha, P Dherbécourt, A El Oualkadi, *Member, IEEE,* Eric Joubert and M Masmoudi

***Abstract*— This paper aims to model the static behavior of two generations of Silicon carbide Metal Oxide Semiconductor Field Effect Transistors (SiC-MOSFETs) subjected to temperature and input voltage variations. The description of the studied device, its electro-thermal characterizations and the comparison of two generations of SiC-MOSFETs are presented. The SPICE model provided by the constructor is studied. The comparison between the simulation results of the SPICE model and measurements reveals limitations in terms of temperature behavior and electrical effects. In order to overcome these limitations, a compact model is used. This model accurately describes the static behavior of two generations of SiC-MOSFETs. The threshold voltage extracted from the compact model is exploited to analyze the physical behavior and to compare the performance of two generations of SiC-MOSFETs.**

***Index Terms*—SiC-MOSFET; Model; Static behavior, Electro-thermal, Physical behavior.**

I. Introduction

Wide bandgap semiconductors, such as Silicon Carbide (SiC) and Nitrite Gallium (GaN), show superior material properties enabling potential power device operation at higher temperatures, voltages, and switching speeds than current Silicon technology, thanks to its wide energy band gap and its higher thermal conductor [1-4]. As a result, SiC metal oxide semiconductor field effect transistors (MOSFETs) offer a way to extend the microelectronic revolution into high temperature and high power applications. The use of these new power semiconductor devices will allow improvement of the performance of power converters, which leads to an increase in the efficiency and a better use of the electric energy [5-6]. However, studies of SiC MOSFET reliability raised significant concerns on the long term operation of these devices, particularly at high temperatures [7-8]. Recently, numerous efforts have been dedicated to develop MOSFET models that are able to precisely describe the static behavior of power transistors, taking into account the specificities of the SiC material and the evolution of electrical parameters under temperature variations. There are two mains models type of SiC MOSFET often used in the literature. The first model is sub-circuit model [9-10]. This model uses a circuit to describe the static behavior of the SiC MOSFET, by adding electronic elements (resistances, diode and capacitances) in order to take into account some physical effects on the transistor operation. The second model is the compact model [11-13]. This model is based on physical equations and it calculates the currents from the voltages applied to the component terminals, and from the physical parameters.

This paper proposes to explore the electro-thermal static behavior and understand the physical parameters variations of power SiC-MOSFETs. In the first time, the SPICE model developed by the CREE constructor has been studied [14], the simulation results based on this model under LTSpice are compared to measurements. Thereafter, a compact model is described and used in order to improve the limits of SPICE model. The threshold voltage extracted from this compact model will be exploited to analyze the static behavior of the transistor, and compare the performance of two generations of SiC-MOSFETs.

This paper is organized as follows. Section II presents the studied devices, their structures and the electro-thermal characterization. Section III describes the SPICE model. Section IV develops the compact model based on physical equation and presents the analysis of the threshold voltage according to the temperature. Finally, the conclusion is given in section V.

II. Description And Electro-thermal Characterization Of Studied Devices

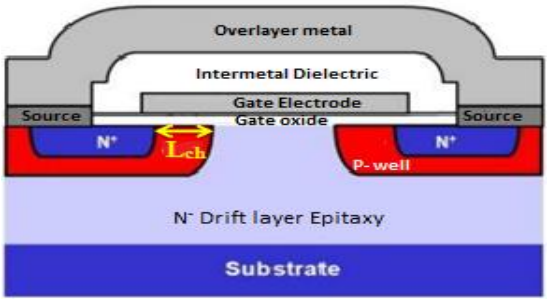
A. Description of the SiC-MOSFETs

The high power SiC-MOSFETs from the CREE Company have been chosen for this study. The second generation of the SiC-MOSFET G2 (10A, 1200V) referenced “C2M0280120D” is compared to the third generation G3 (11A, 900V) referenced “C3M0280090D” [15-16]. The choice of these two generations is based on the fact that both references have approximately similar nominal drain currents. Figure 1 shows the physical structures of the two generations. The devices are n-channel vertical D-MOSFETs (double-diffused MOS) with

W. Jouha is with the Laboratory of Information Technology and Communication, National School of Applied Sciences of Tangier. University Abdelmalek Essaadi Tétouan, Maroc, and he is with Normandie Université, UNIROUEN, INSA Rouen, CNRS, Groupe de Physique des Matériaux, UMR 6634, Avenue de l’université B.P 12, 76800, France (jouhaieea@gmail.com).

A. El Oualkadi is with the Laboratory of Information Technology and Communication, National School of Applied Sciences of Tangier. University Abdelmalek Essaadi Tétouan, Maroc (eloualkadi@gmail.com).

P. Dherbécourt, E. Joubert and M. Masmoudi are with Normandie Université, UNIROUEN, INSA Rouen, CNRS, Groupe de Physique des Matériaux, UMR 6634, Avenue de l’université B.P 12, 76800, France (pascal.dherbecourt@univ-rouen.fr, eric.joubert@univ-rouen.fr, mohamed.masmoudi@univ-rouen.fr).



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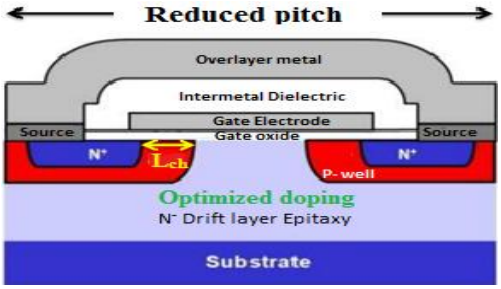


(b)

Fig. 1. MOSFET structure: (a) second generation (G2), and (b) third generation (G3) [17].

SiC substrate. The constructor maintains the same planar structure for the two generations of MOSFETs. However, the doping is optimized for the third generation. Moreover, the pitch is reduced as well as the epitaxy thickness, and the gate width. These improvements increase the maximum operating temperatures which reduce the size of the cooling devices required in energy conversion systems.

B. Electro-Thermal Characterization

From each generation, a sample transistor is selected to be characterized. For this purpose, the static I-V characterizations have been performed using a bench generating a pulse measurement duration not exceeding 7 µs in order to limit the self-heating of the device under test. The measurements are conducted over a temperature range from 0°C to 135°C. The temperature is controlled by a Peltier module.

The input characteristics (I_{ds} = f (V_{gs})) and the output characteristics (I_{ds} = f (V_{ds})) are measured for both MOSFET generations for various values of V_{ds} and V_{gs} respectively. Figure 2 shows the input characteristics, while Figure 3 shows the output characteristics.

These electro-thermal characterizations allow the extraction of the MOSFET electrical parameters: the transconductance g_m and the on-state resistance $R_{ds(on)}$. These parameters are used to study the behavior of the transistor as a function of temperature and compare the two generations transistors. The transconductance g_m represents the image of the effective electron mobility in the channel according to the following equation [18]:

$$g_m = \frac{N_{cell}.Z.C_{ox}.\mu_n}{L_{ch}} V_{ds} \quad (1)$$

Where, N_{cell} is the number of transistor cells, Z is the length of a cell, C_{ox} is the gate oxide capacitance and L_{ch} is the channel length. The transconductance is calculated from the input characteristics $g_m = (\Delta I_{ds}/\Delta V_{gs})$. Figure 4 shows the transconductance as a function of the input voltage V_{gs} for various temperatures.

For both generations, the transconductance g_m rises with the increase of the temperature and the input voltage V_{gs}, up to a critical voltage V_{gs} where g_m decreases with the increasing temperature. This critical point is named "Zero Temperature Coefficient" (ZTC). It is related to the dependence of the electron mobility to the temperature and the transversal electric field generated by the input voltage V_{gs} [19]. The ZTC point appears at V_{gs} = 9V for the third generation before that

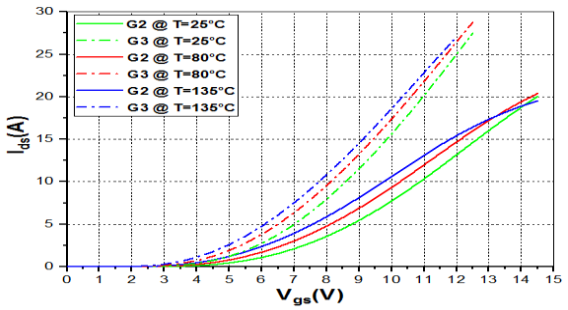
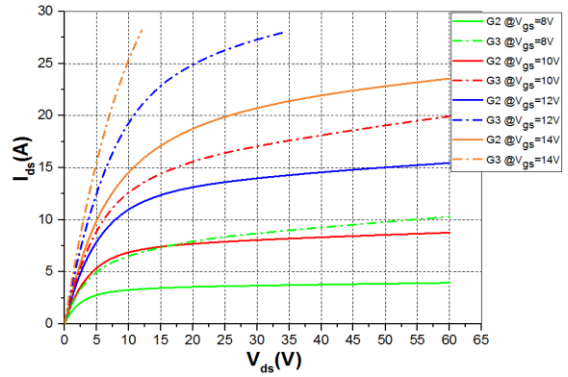


Fig. 2. Input characteristics for V_{ds}=18V, at three temperatures (25°C, 80°C and 135°C) for two generations G2 (solid) and G3 (dashed).



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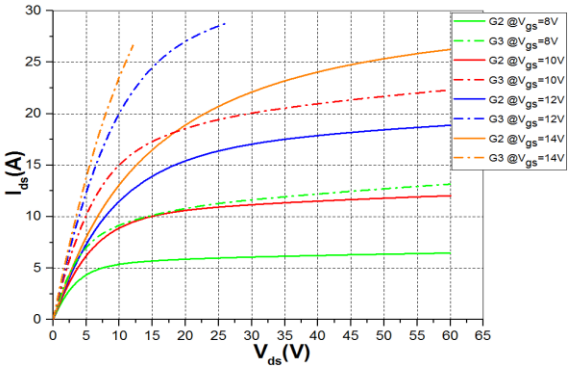

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Fig. 3. Output characteristics for V_{gs} (8V, 10V, 12V and 14V), and for two generations G2 (solid) and G3 (dashed), at two temperatures: (a) 25°C, and (b) 135°C.

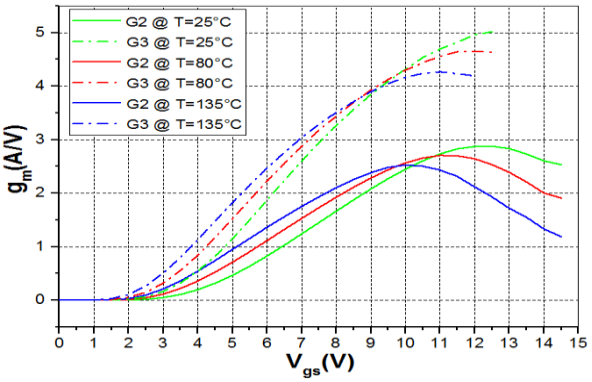


Fig. 4. Transconductance g_m as a function of V_{gs} at three temperatures (25°C, 80°C and 135°C) for two generations G2 (solid) and G3 (dashed).

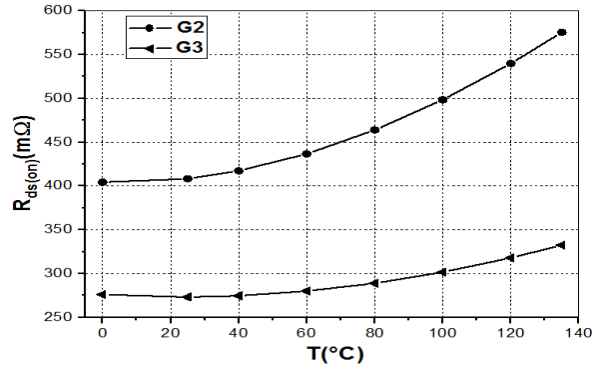


Fig. 5. On-state resistance $R_{ds(on)}$ as function of temperatures at V_{ds}= 20V for two generations G2 and G3.

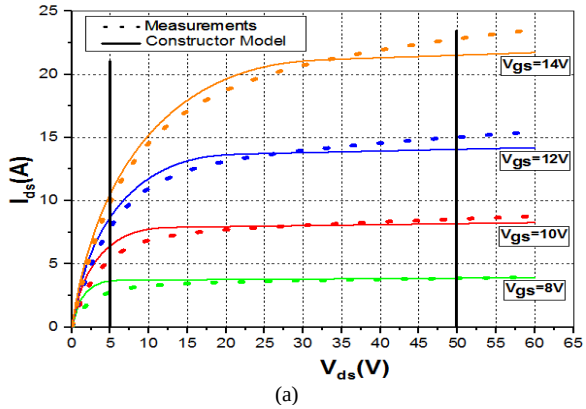
of the second generation which appears at V_{gs} = 10V. This can be justified by the low threshold voltage, extracted from datasheet, for the third generation.

Considering the output characteristics, the definition of the on-state resistance $R_{ds(on)}$ is necessary to identify the power losses of the MOSFET in conduction. This resistance represents the variation of output voltage V_{ds} divided by the output current I_{ds} ($R_{ds(on)} = (\Delta V_{ds}/\Delta I_{ds})$). The $R_{ds(on)}$ is calculated for I_{ds} = 5A and V_{gs} = 14V for various temperature values between 0°C and 135°C. Figure 5 shows the $R_{ds(on)}$ as a function of temperature for the two generations.

The two generations have the same behavior of $R_{ds(on)}$ as a function of temperature. The $R_{ds(on)}$ rises with the increase of temperature [20-21]. However, the $R_{ds(on)}$ value for the third generation is less than that of the second generation. This is due to the size reduction of oxide thickness and gate width of the third generation structure.

III. SPICE MODEL OF SIC-MOSFET

The constructor provides a SPICE model for his transistors. The simulation of this model is performed under LTSpice tool. Figures 6 and 7 show the comparisons of the output characteristics between the simulation results of SPICE model and measurements for two generations of SiC-MOSFET. However, Tables I and II show the relative variations between the SPICE model and measurements for the two generations of SiC-MOSFET at two values of V_{ds} (5V and 50V). The



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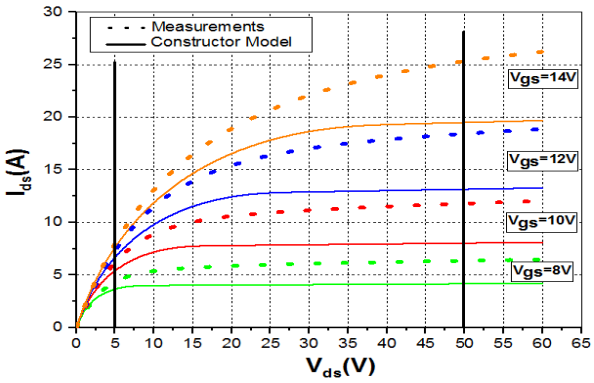

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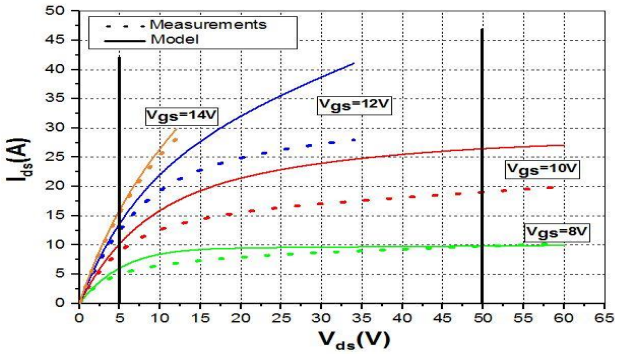
Fig. 6. The comparison of the output characteristics between the simulation results of SPICE model and measurements of the second generation of SiC-MOSFET at two temperatures: (a) 25°C, and (b) 135°C.



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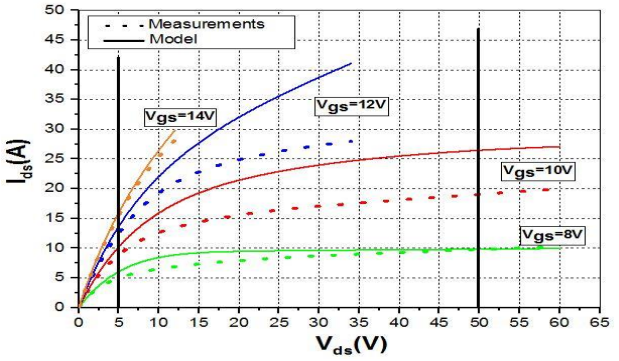

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Fig. 7. Comparison of the output characteristics between the simulation results of SPICE model and measurements of the third generation of

TABLE I
RELATIVE VARIATIONS BETWEEN THE SPICE MODEL RESULTS AND MEASUREMENTS FOR SECOND GENERATION

Temperature	25°C		135°C	
V_{ds} / V_{gs}	5V	50V	5V	50V
8V	24.31 %	0 %	15.27 %	34.64 %
10V	16.87 %	4.32 %	12.45 %	31.89 %
12V	10.09 %	6.38 %	8.85 %	28.64 %
14V	6.53 %	5.74 %	4.26 %	23.04 %

TABLE II
RELATIVE VARIATIONS BETWEEN THE SPICE MODEL RESULTS AND MEASUREMENTS FOR THIRD GENERATION

Temperature	25°C		135°C	
V_{ds} / V_{gs}	5V	50V	5V	50V
8V	25.82 %	0.5 %	0.98 %	4.8 %
10V	13.56 %	28.01 %	3.54 %	17.78 %
12V	8.69 %	-	4.24 %	-
14V	3.18 %	-	7.25 %	-

absence of measurements values in Table II for V_{gs} = 12V and V_{gs} = 14V at V_{ds} = 50V is due to the current limitation of the measuring probe (I_{dsmax} = 28A). The relative variation of I_{ds} is calculated by:

$$Relative\ variation = \left(\frac{I_{ds(sim)} - I_{ds(mes)}}{I_{ds(sim)}} \right) \times 100 \qquad (2)$$

Where, $I_{ds(sim)}$ is the simulation value of I_{ds} and $I_{ds(mes)}$ is the measurement value of I_{ds}.

The comparison of these results shows significant disparities between the SPICE model and the measurements. The exploitation of the SPICE model shows an insufficient dependence of the temperature effects on the static behavior of the transistor. The parameters of constructor model have fixed values and they are not taking into account the variation of the electrical and physical parameters of the transistor (threshold voltage, effective mobility of electrons) as a function of temperature and the voltages applied to its terminals (V_{ds} and V_{gs}). These limitations make this model incompatible with the use of these components under operational conditions at various temperatures [21]. In fact, the SPICE model is only useful for the circuit design on the simulation tools. Hence, the need to use another model based on physical equations which can be more flexible, precise and can take into account the evolution of electrical parameters with temperature.

IV. COMPACT MODEL OF SIC MOSFET

In order to overcome the limitations of the SPICE model, we use a compact model presented in [22]. This model describes the output current I_{ds} in two operating regimes by the following equations:

- Linear regime ($0 \le V_{ds} \le \frac{Vgs-Vth}{P_{vf}}$):

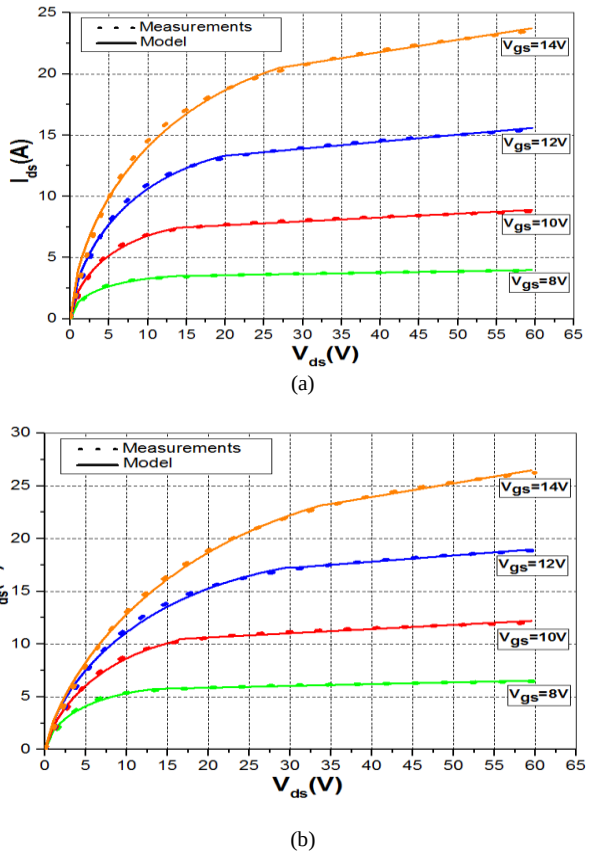

Fig. 8. Comparison of the output characteristics between the compact model and the measurements of the second generation of SiC MOSFET at two temperatures: (a) 25 °C, and (b) 135 °C.

$$I_{ds} = \frac{K_f K_p}{1+\theta(V_{gs}-V_{th})} \left[(V_{gs}-V_{th})V_{ds} - \frac{P_{vf}^{y-1} V_{ds}^{y} (V_{gs}-V_{th})^{2-y}}{y} \right] \qquad (3)$$

- Saturation regime ($0 \le \frac{Vgs-Vth}{P_{vf}} \le V_{ds}$):

$$I_{ds} = \frac{K_p (V_{gs}-V_{th})^2}{2(1+\theta(V_{gs}-V_{th}))} (1+\lambda V_{ds}) \qquad (4)$$

Where, K_p is the saturation region transconductance expressed in (A/V^2). The parameter θ is an empirical correction factor (V^{-1}) introduced to take into account the mobility reduction. P_{vf} and K_f are two correction factors for the pinch voltage and the K_p respectively, λ is the coefficient of the channel modulation effect, and y is an exponent. The extraction of the model parameters is based on the use of static measurements I-V in pulsed mode with the Levenberg-Marquardt optimization algorithm [23-24].

The compact model has been exploited to describe the static behavior of two generations of SiC MOSFET according to the temperature. Figures 8 and 9 show the output curves of the compact model compared to measurements for two generations of SiC MOSFET. Tables III and IV show relative variations between measurements and simulation results of the compact model for the two generations.

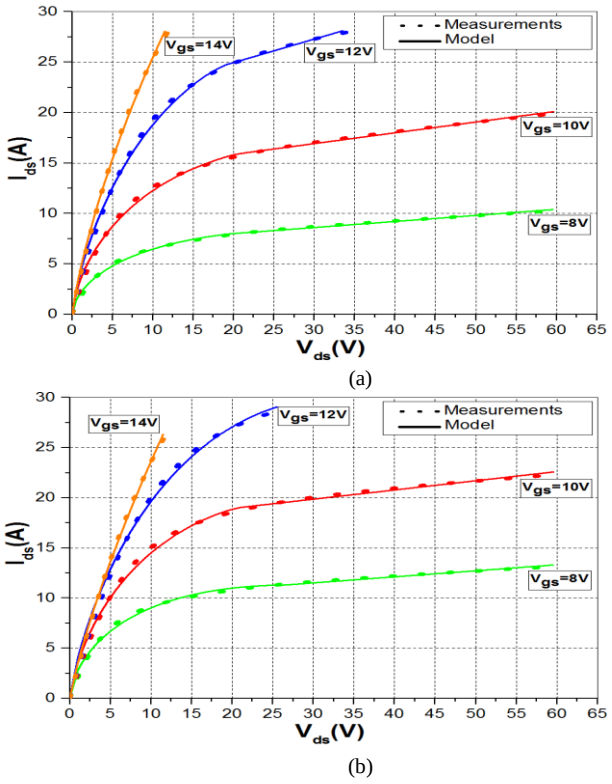

Fig. 9. Comparison of the output characteristics between the compact model and the measurements of the third generation of SiC MOSFET at two temperatures: (a) 25 °C, and (b) 135 °C.

TABLE III
RELATIVE VARIATIONS BETWEEN THE COMPACT MODEL RESULTS AND MEASUREMENTS FOR SECOND GENERATION

Temperature	25°C		135°C	
V_{ds} / V_{gs}	5V	50V	5V	50V
8V	4.69 %	0 %	4.86 %	0.15 %
10V	4.09 %	1.16 %	1.77 %	0.16 %
12V	1.53 %	0.06 %	3.32 %	0.1 %
14V	0.6 %	0.13 %	3.74 %	0.43 %

TABLE IV
RELATIVE VARIATIONS BETWEEN THE COMPACT MODEL RESULTS AND MEASUREMENTS FOR THIRD GENERATION

Temperature	25°C		135°C	
V_{ds} / V_{gs}	5V	50V	5V	50V
8V	3.62 %	0.2 %	0.03 %	1.57 %
10V	1.69 %	0.01 %	1.18 %	0.09 %
12V	0.47 %	-	4.66 %	-
14V	1.03 %	-	1.45 %	-

The results show that the compact model is more accurate and matches very well the measurements. The difference between the simulation results of the compact model and measurements is very lower compared to the obtained results using the SPICE model (Table I and Table II). The obtained results show the efficiency of the compact model on the temperature range from 0°C to 135°C and for various values of the voltage V_{gs}.

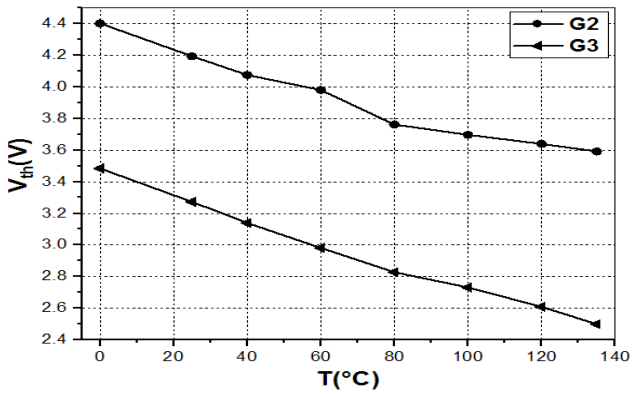

Fig. 10. Threshold voltage V_{th} as function temperature at V_{ds} =20 V for two generations G2 and G3.

One of the important parameters extracted from the compact model is the threshold voltage V_{th}. Figure 10 shows the evolution of threshold voltage V_{th} as a function of temperature for two generations of SiC MOSFET.

From Figure 10, it is observed that V_{th} decreases when the temperature increases for two generations of SiC MOSFET. Indeed, the increase of temperature causes the appearance of charges in the oxide and the decrease of the N channel resistance [25]. Physically, the relation between V_{th} and temperature is given by [18]:

$$V_{th} = \frac{\sqrt{4\varepsilon_{sic} k T_j N_A \ln\left(\frac{N_A}{n_i}\right)}}{C_{ox}} + \frac{2KT_j}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{ox}}{C_{ox}} \qquad (5)$$

Where, $C_{ox}=(3.9\ \varepsilon_0/\ t_{ox})$ is the gate oxide capacitance, ε_0 and ε_{SiC} are the permittivity for the vacuum and the semi-conductor SiC respectively, t_{ox} is the oxide thickness, Q_{ox} is the total effective charge in the oxide, N_A is the doping concentration of N, et n_i is the intrinsic carrier concentration.

The equation 5 shows the dependence of V_{th} on temperature and the physical parameters of transistor particularly N_A and C_{ox}. Since the third generation has an optimized doping and a reduced oxide thickness compared to the second generation, the V_{th} of the third generation is reduced compared to the second generation.

V. CONCLUSION

This study aims to characterize and to model the static behavior of two generations of SiC-MOSFETs. We investigated the behavior of their relevant parameters (transconductance g_m and on-state resistance $R_{ds(on)}$) as a function of the temperature and the input voltage input V_{gs}.. The comparison between the simulation results based on constructor's SPICE model and the measurements shows significant differences. These dispersions are justified by the limitation of SPICE model in terms of thermal and electrical constraints. A compact model based on the physical equations of the component overcomes these limitations. This model describes accurately and efficiently the static behavior of the

transistors as a function of temperature and input voltage variations. The exploitation of threshold voltage extracted from the compact model shows that the static behavior of the component is highly dependent of the temperature variations and physical parameters of the device such as oxide capacitance and doping concentration.

The compact model is an effective tool for future works to evaluate the reliability of these MOSFETs and the interpretation of data resulting from aging tests, in order to identify and understand the failure mechanisms of SiC technology.

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